AMENDMENTS TO THE CLAIMS

A complete set of the existing claims are set forth below, with the amended claims showing deletions, (strikethrough) and insertions (underline).

1. (Currently amended) A two-transistor DRAM cell comprising:

a NMOS device with a first gate; ~~and~~

a PMOS device with a second gate, the PMOS device coupled to the NMOS device~~.~~; and

a storage node coupled to at least one of the first and the second gates.

2. (Currently amended) The two-transistor DRAM cell of claim 1, wherein ~~a~~ the storage node is defined between the PMOS device and the NMOS device, the storage node having a voltage that converges to Vhigh, where Vhigh is greater than Vcc/2.

3. (Original) The two-transistor DRAM cell of claim 1, further comprising:

an n-channel (NMOS) device coupled between the read bit line and the read word line; and

a p-channel (PMOS) device coupled to the NMOS device so as to define a storage node therebetween.

4. (Original) A DRAM cell comprising:

a read bit line;

a write bit line;

a read word line;

a write word line;

an n-channel (NMOS) device coupled between the read bit line and the read word line; and

a p-channel (PMOS) device coupled to the NMOS device so as to define a storage node therebetween.

5. (Original) The DRAM cell of claim 4, wherein the PMOS device is coupled between the write bit line and a gate region of the NMOS device.

6. (Original) The DRAM cell of claim 5, wherein the PMOS device comprises a gate region coupled to the write word line.

7. (Original) The DRAM cell of claim 4, wherein the write word line is pulled from a logic high voltage to a logic low voltage to write data into the DRAM cell.

8. (Original) The DRAM cell of claim 7, wherein the read word line, the read bit line and the write word line are held at a logic high voltage to hold data within the DRAM cell.

9. (Original) The DRAM cell of claim 7, wherein the data written into the DRAM cell corresponds to the voltage level of the write bit line.

10. (Original)The DRAM cell of claim 4, wherein a voltage level of the storage node converges to logic high due to edge leakage current.

11. (Original) A DRAM cell comprising:

a read bit line;

a write bit line;

a read word line;

a write word line;

a p-channel (PMOS) device coupled between the read bit line and the read word line; and

an n-channel (NMOS) device coupled between the write bit line and a gate region of the PMOS device so as to form a storage node therebetween.

12. (Original) The DRAM cell of claim 11, wherein the NMOS device comprises a gate region coupled to the write word line.

13. (Original) The DRAM cell of claim 11, wherein the NMOS device is coupled to the write word line.

14. (Original) The DRAM cell of claim 13, wherein the write word line is pulled from a logic low voltage to a logic high voltage to write data into the DRAM cell.

15. (Original) The DRAM cell of claim 13, wherein the read word line, the read bit line and the write word line are held at a logic low voltage to hold data within the DRAM cell.

16. (Original) The DRAM cell of claim 13, wherein the data written into the DRAM cell corresponds to the voltage level of the write bit line.

17. (Original) The DRAM cell of claim 11, wherein a voltage level of the storage node converges to logic high due to edge leakage current.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Currently amended) A system comprising:
an integrated circuit (IC); and
memory coupled to the IC, the memory including at least one two-transistor DRAM cell having
a NMOS device with a first gate; ~~and~~
a PMOS device with a second gate, the PMOS device coupled to the NMOS device~~.~~; and
a storage node coupled to at least one of the first and the second gates.

22. (Original) The system according to claim 21, wherein the IC comprises a central processing unit, and at least one input/output module coupled to the central processor unit.

23. (Original) The system of claim 21, wherein the memory is coupled to the IC via the communication channel.